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DUAL EPITAXIAL LAYER FOR HIGH VOLTAGE VERTICAL CONDUCTION POWER MOSFET DEVICES

ABSTRACT OF THE DISCLOSURE

The epitaxial silicon junction receiving layer of a power semiconductor device is formed of upper and lower layers. The lower layer has a resistivity of more than that of the upper layer and a thickness of more than that of the upper layer. The total thickness of the two layers is less than that of a single epitaxial layer that would be used for the same blocking voltage. P-N junctions are formed in the upper layer to define a vertical conduction power MOSFET device. The on-resistance is reduced more than 10% without any blocking voltage reduce. The upper epitaxial layer can be either by direct second layer deposition or by ion implantation of a uniform epitaxial layer followed by a driving process.